Remarks

The Office Action of June 4, 2002 has been received and reviewed. With claims 58, 66, 74, 83, 93, and 102 having been amended, the pending claims remain claims 58-105. Reconsideration and withdrawal of the rejections are respectfully requested for at least the reasons set forth below.

The 35 U.S.C. §112, First Paragraph, Rejection

Claims 59, 60, 67, 68, 74, 85, 86, 94, 95, 103, and 104 were rejected under 35 U.S.C. § 112, first paragraph, as containing subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention.

With respect to claims 59, 67, 85, 94, and 103, the Office Action alleges that the recitation of a conductive metal layer having a thickness of 600 Å or less introduces new matter. In addition, the Office Action alleges that a conductive metal layer having a thickness of 500 Å or less, as recited in claims 60, 68, 86, 95, and 104, also introduces new matter (Applicant notes that claim 104, contrary to the assertions of the Office Action, does not recite layer thickness). Still further, with reference to claim 74, the Office Action alleges that the recitation of annealing the substrate assembly at a temperature of about 1100 °C or less also introduces new matter. Applicant traverses.

The specification clearly describes a conductive metal layer, e.g., platinum, having a thickness of "about 600 Å or less" (see e.g., page 3, line 22; page 4, line 27; page 13, line 4; page 15, line 7; now-canceled claim 2), and having a thickness of "about 500 Å or less" (see e.g., page 4, lines 27-28; page 13, line 5; now-canceled claim 3). Similarly, the specification clearly describes annealing the substrate assembly at a temperature of "about 1100°C or less" (see e.g., page 3, line 22-23; now-canceled claim 25).

Because these recitations are clearly described in the specification, no new matter has been introduced. Accordingly, withdrawal of the rejection is requested.

The 35 U.S.C. §102 Rejection

Claims 58-61, 63-69, 71-74, 76, 78-80, 83-86, 88, 90-96, and 98-105 were rejected under 35 U.S.C. § 102(b) as being anticipated by Nishioka et al. (U.S. Patent No. 5,489,548). Applicant traverses for at least the following reasons.

Independent claims 58, 66, 74, 83, 93, and 102, have been amended to require, for example, annealing the substrate assembly including the metal-containing adhesion layer and the conductive layer thereon, causing pooling of the conductive layer on at least one exposed surface region of the substrate assembly. Pooling is described in the specification, see e.g., page 5, lines 25-29. Claims 58, 66, 83, and 93 have also been amended to remove recitations not necessary to distinguish the respective claims over the cited art.

There is no disclosure identified in Nishioka et al. of pooling of the conductive layer on an exposed surface of the substrate assembly as claimed. Accordingly, these independent claims are submitted to be novel in view of Nishioka et al. The claims that depend therefrom are also considered novel both in view of their dependence on these claims and further in view of the particular features addressed therein. Reconsideration of claims 58-61, 63-69, 71-74, 76, 78-80, 83-86, 88, 90-96, and 98-105 and withdrawal of the rejection are respectfully requested.

The 35 U.S.C. §103 Rejection

Claims 62, 70, 77, 89, and 97 were rejected under 35 U.S.C. §103(a) as being unpatentable over Nishioka et al. in view of Huffman (U.S. Patent No. 5,191,510). Claims 75 and 87 were rejected under 35 U.S.C. §103(a) as being unpatentable over Nishioka et al. Claims 81 and 82 were rejected under 35 U.S.C. §103(a) as being unpatentable over Nishioka et al. in view of DeOrnellas et al. (U.S. Patent No. 6,127,277).

For the reasons enumerated above, Nishioka et al. fails to teach the elements of the claims as asserted by the Office Action. There is nothing identified in Huffman and DeOrnellas

et al. that addresses these shortcomings. Therefore, reconsideration and withdrawal of these 35 U.S.C. § 103(a) rejections are requested.

Summary

It is submitted that pending claims 58-105 are in condition for allowance and notification to that effect is respectfully requested. The Examiner is invited to contact Applicant's Representatives, at the below-listed telephone number, if it is believed that prosecution of this application may be assisted thereby.

CERTIFICATE UNDER 37 CFR §1.10:
"Express Mail" mailing
label number: EV 183606408 US
Date of Deposit: September 4, 2002
The undersigned hereby certifies that this paper is being deposited with the United States Postal Service "Express Mail Post Office to Addressee" service under 37 C.F.R. § 1.10 on the date indicated above and is addressed to the Assistant Commissioner for Patents, Washington, D.C. 20231.

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APPENDIX A - SPECIFICATION/CLAIM AMENDMENTS INCLUDING NOTATIONS TO INDICATE CHANGES MADE
Serial No.:09/812,157
Docket No.: 150.00930102

Amendments to the following are indicated by underlining what has been added and bracketing what has been deleted.

In the Specification

The Abstract beginning at page 37, line 6, has been amended as follows:

The present invention provides a method for forming a discontinuous conductive layer in the fabrication of integrated circuits. The method includes providing a substrate assembly having a surface including at least one metal-containing adhesion region separated by at least one surface region of the substrate assembly. A conductive metal layer is formed on the surface of the substrate assembly. The substrate assembly including the conductive metal layer thereon [in] is then annealed. Any nonadhered conductive metal is removed from the at least one exposed surface region to form a discontinuous conductive metal layer on at least one metal-containing adhesion region, for example, by simply [rising] rinsing the substrate assembly in water. The conductive metal layer can be platinum or ruthenium.

In the Claims

For convenience, all pending claims are shown below.

58. **(AMENDED)** A method for patterning a platinum layer in the fabrication of integrated circuits, the method comprising:

providing a substrate assembly including a surface;

forming a patterned metal-containing adhesion layer on the surface, resulting in at least one exposed surface region of the substrate assembly;

forming platinum on the patterned metal-containing adhesion layer and the at least one exposed surface region of the substrate assembly;

annealing the substrate assembly including the patterned metal-containing adhesion layer and the platinum thereon, causing pooling of the platinum on the at least one exposed surface region of the substrate assembly; and

removing at least a portion of the platinum from the at least one exposed surface region of the substrate assembly resulting in a patterned platinum layer [, wherein annealing the substrate assembly and removing the portion of the platinum from the at least one exposed surface region is performed prior to forming any other materials on the platinum].

59. The method of claim 58, wherein forming the platinum comprises forming the platinum layer having a thickness of about 600 Å or less.

60. The method of claim 59, wherein forming the platinum comprises forming the platinum layer having a thickness of about 500 Å or less.

61. The method of claim 58, wherein annealing the substrate assembly comprises annealing the substrate assembly at a temperature less than the melting point of the at least one exposed surface region.

62. The method of claim 58, wherein annealing the substrate assembly comprises performing a rapid thermal anneal in an atmosphere of at least one of oxygen and nitrogen.

63. The method of claim 58, wherein the patterned metal-containing adhesion layer comprises at least one material selected from the group consisting of titanium, tantalum, tungsten, rhodium, iridium, cobalt, and nitrides, oxides, and silicides thereof.

64. The method of claim 58, wherein the patterned metal-containing adhesion layer comprises titanium nitride.

65. The method of claim 58, wherein the at least one exposed surface region comprises at least one material selected from the group consisting of silicon, silicon dioxide, BPSG, PSG, Al_2O_3, and combinations thereof.

66. **(AMENDED)** A method for forming a discontinuous conductive layer in the fabrication of integrated circuits, the method comprising:

providing a substrate assembly comprising a surface having at least one metal-containing adhesion region and at least one surface region;

forming a platinum layer on the surface of the substrate assembly;

annealing the substrate assembly including the platinum layer formed thereon, causing pooling of the platinum layer on the at least one surface region of the substrate assembly; and

removing at least a portion of the platinum layer from the at least one surface region resulting in a discontinuous platinum layer on the at least one metal-containing adhesion region [, wherein annealing the substrate assembly and removing the portion of the platinum layer from the at least one surface region is performed prior to forming any other materials on the platinum layer].

67. The method of claim 66, wherein forming the platinum layer comprises forming the platinum layer having a thickness of about 600 Å or less.

68. The method of claim 67, wherein forming the platinum layer comprises forming the platinum layer having a thickness of about 500 Å or less.

69. The method of claim 66, wherein annealing the substrate assembly comprises annealing the substrate assembly at a temperature less than the melting point of the at least one surface region.

70. The method of claim 66, wherein annealing the substrate assembly comprises performing a rapid thermal anneal in an atmosphere of at least one of oxygen and nitrogen.

71. The method of claim 66, wherein the at least one metal-containing adhesion region comprises at least one material selected from the group consisting of titanium, tantalum, tungsten, rhodium, iridium, cobalt, and nitrides, oxides, and silicides thereof.

72. The method of claim 66, wherein the at least one metal-containing adhesion region comprises titanium nitride.

73. The method of claim 66, wherein the at least one surface region comprises at least one material selected from the group consisting of silicon, silicon dioxide, BPSG, PSG, Al_2O_3, and a combination thereof.

74. **(AMENDED)** A method for forming a patterned platinum layer in the fabrication of integrated circuits, the method comprising:

providing a substrate assembly including a surface having a patterned metal-containing adhesion portion thereon;

depositing a platinum layer on the surface of the substrate assembly and the patterned metal-containing adhesion portion, wherein the platinum layer has a thickness of about 600 Å or less;

annealing the substrate assembly at a temperature of about 1100°C or less, causing pooling of the platinum layer on the surface of the substrate assembly; and

removing unadhered platinum from at least a portion of the surface of the substrate assembly such that a resulting patterned platinum layer has a configuration substantially that of the patterned metal-containing adhesion portion, wherein annealing the substrate assembly and

removing unadhered platinum from the portion of the surface of the substrate assembly is performed prior to forming any other materials on the platinum layer.

75. The method of claim 74, wherein the temperature is between about 650°C and about 1100°C.

76. The method of claim 74, wherein annealing the substrate assembly occurs in an atmosphere comprising at least one compound selected from the group consisting of oxygen, ozone, nitrogen, argon, NO_x, SO_3, N_2O, and combinations thereof.

77. The method of claim 74, wherein annealing the substrate assembly comprises performing a rapid thermal anneal in an atmosphere of at least one of oxygen and nitrogen.

78. The method of claim 74, wherein the at least one patterned metal-containing adhesion portion comprises at least one material selected from the group consisting of titanium, tantalum, tungsten, rhodium, iridium, cobalt, and nitrides, oxides, and silicides thereof.

79. The method of claim 74, wherein the at least one patterned metal-containing adhesion portion comprises titanium nitride.

80. The method of claim 74, wherein the surface of the substrate assembly comprises at least one material selected from the group consisting of silicon, silicon dioxide, BPSG, PSG, Al_2O_3, and combinations thereof.

81. The method of claim 74, wherein removing unadhered platinum comprises rinsing the substrate assembly in a rinsing composition for a period of time of about 5 minutes or less.

82. The method of claim 81, wherein the rinsing composition comprises at least one composition selected from the group consisting of water, aqua regia, hydrofluoric acid, hydrochloric acid, hydrogen peroxide, and combinations thereof.

83. **(AMENDED)** A method for use in forming a capacitor, the method comprising:

providing a substrate assembly, the substrate assembly including at least one surface; and

forming an electrode on the at least one surface of the substrate assembly, wherein forming the electrode comprises at least forming a platinum electrode layer, wherein forming the platinum electrode layer comprises:

forming a discontinuous metal-containing adhesion layer on the at least one surface;

forming a platinum layer on at least portions of the at least one surface of the substrate assembly and the discontinuous metal-containing adhesion layer;

annealing the substrate assembly, causing pooling of the platinum layer on portions of the at least one surface of the substrate assembly; and

removing at least a portion of the platinum layer from the at least one surface of the substrate assembly resulting in a discontinuous platinum layer [, wherein annealing the substrate assembly and removing the at least a portion of the platinum layer from the at least one surface of the substrate assembly is performed prior to forming any other materials on the platinum].

84. The method of claim 83, wherein the substrate assembly includes an opening defined therein, wherein the opening is defined by a bottom surface of the substrate assembly and at least one side wall surface extending therefrom and further wherein the discontinuous metal-containing adhesion layer is formed on the surfaces defining the opening.

85. The method of claim 83, wherein the platinum layer has a thickness of about 600 Å or less.

86. The method of claim 85, wherein the platinum layer has a thickness of about 500 Å or less.

87. The method of claim 83, wherein annealing the substrate assembly comprises annealing the substrate assembly at a temperature between about 650°C and about 1100°C.

88. The method of claim 83, wherein annealing the substrate assembly occurs in an atmosphere comprising at least one compound selected from the group consisting of oxygen, ozone, nitrogen, argon, NO_x, SO_3, N_2O, and combinations thereof.

89. The method of claim 83, wherein annealing the substrate assembly comprises performing a rapid thermal anneal in an atmosphere of at least one of oxygen and nitrogen.

90. The method of claim 83, wherein the discontinuous metal-containing adhesion layer comprises at least one material selected from the group consisting of titanium, tantalum, tungsten, rhodium, iridium, cobalt, and nitrides, oxides, and silicides thereof.

91. The method of claim 83, wherein the discontinuous metal-containing adhesion layer comprises titanium nitride.

92. The method of claim 83, wherein the at least one surface of the substrate assembly comprises at least one material selected from the group consisting of silicon, silicon dioxide, BPSG, PSG, Al_2O_3, and a combination thereof.

93. **(AMENDED)** A method for forming a discontinuous conductive layer in the fabrication of integrated circuits, the method comprising:

providing a substrate assembly having a surface comprising at least one metal-containing adhesion region and at least one surface region;

forming a conductive metal layer on the surface of the substrate assembly, wherein the conductive metal layer comprises a metal different from a metal in the at least one metal-containing adhesion region;

annealing the substrate assembly including the conductive metal layer, causing pooling of the conductive metal layer on the at least one surface region of the substrate assembly; and

removing at least a portion of the conductive metal layer from the at least one surface region resulting in a discontinuous conductive metal layer on the at least one metal-containing adhesion region [, wherein annealing the substrate assembly and removing the at least a portion of the conductive metal layer from the at least one surface region is performed prior to forming any other materials on the conductive metal layer].

94. The method of claim 93, wherein forming the conductive metal layer comprises forming the conductive metal layer having a thickness of about 600 Å or less.

95. The method of claim 94, wherein forming the conductive metal layer comprises forming the conductive metal layer having a thickness of about 500 Å or less.

96. The method of claim 93, wherein annealing the substrate assembly comprises annealing the substrate assembly at a temperature less than the melting point of the at least one surface region.

97. The method of claim 93, wherein annealing the substrate assembly comprises performing a rapid thermal anneal in an atmosphere of at least one of oxygen and nitrogen.

98. The method of claim 93, wherein the at least one metal-containing adhesion region comprises at least one material selected from the group consisting of titanium, tantalum, tungsten, rhodium, iridium, cobalt, and nitrides, oxides, and silicides thereof.

99. The method of claim 93, wherein the at least one metal-containing adhesion region comprises titanium nitride.

100. The method of claim 93, wherein the at least one surface region comprises at least one material selected from the group consisting of silicon, silicon dioxide, BPSG, PSG, and Al_2O_3.

101. The method of claim 93, wherein the conductive metal layer comprises at least one metal selected from the group consisting of platinum or ruthenium.

102. **(AMENDED)** A method for patterning a platinum layer in the fabrication of integrated circuits, the method comprising:

providing a substrate assembly including a surface;

forming a titanium nitride layer on the surface of the substrate assembly;

patterning the titanium nitride layer to form a patterned titanium nitride adhesion layer on the surface, wherein patterning the titanium nitride layer results in at least one exposed surface region of the substrate assembly;

depositing a material comprising platinum on the patterned titanium nitride adhesion layer and the at least one exposed surface region of the substrate assembly;

annealing the substrate assembly including the patterned titanium nitride adhesion layer and the material comprising platinum, causing pooling of the material comprising platinum on the at least one exposed surface region of the substrate assembly; and

removing at least a portion of the material comprising platinum from the at least one exposed surface region of the substrate assembly resulting in a patterned platinum layer.

103. The method of claim 102, wherein depositing the material comprising platinum comprises depositing a platinum layer having a thickness of about 600 Å or less.

104. The method of claim 102, wherein depositing the material comprising platinum comprises depositing a platinum layer using a chemical vapor deposition process.

105. The method of claim 102, wherein depositing the material comprising platinum comprises depositing a platinum layer consisting essentially of platinum.